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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/780,393 | 02/17/2004 | David M. Fried | BUR920010162US1 | 1627 |

30449 7590 03/02/2006

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| EXAMINER | |
|---|---|
| WILSON, SCOTT R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

10

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/780,393 | FRIED ET AL. | |
| | Examiner | Art Unit | |
| | Scott R. Wilson | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-12,14 and 23-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-29* is/are allowed.

6)☒ Claim(s) *9-11,14,23-25 and 30* is/are rejected.

7)☒ Claim(s) *12 and 31-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

dc Minhloan Tran

***Minhloan Tran***
***Primary Examiner***
***Art Unit 2826***

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic et al. in view of Kumar. As to claim 9, Krivokapic et al., Figures 16a and 16b, discloses a method for forming a semiconductor device, the method comprising the steps of: providing a semiconductor substrate (106), patterning the semiconductor substrate to provide a body (242), the body having a first side and a second side, forming a first double gate, the first double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side. Krivokapic et al. does not disclose expressly a second double gate. Kumar, Figure 4, discloses a dual double gate FET embodied as a microwave frequency power divider. The double gate of Kumar would necessarily be embodied by a pair of adjacent double gates in the device of Krivokapic et al., which would necessarily have the second double gate having a first portion adjacent to the body first side and a second portion adjacent to the said body second side the first portion of the first double gate having a surface that is coplanar with a surface of the first portion of the second double gate the second portion of the first double gate having a surface that is coplanar with a surface of the second portion of the second double gate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to

form an additional double gate, of the same form and structure as the disclosed double gate, in the device of Krivokapic et al. in order to fabricate the circuit of Kumar. The motivation for doing so would have been to construct a device which can divide a power signal among two or more paths (Kumar, col. 1, lines 14-15). Therefore, it would have been obvious to combine Kumar with Krivokapic et al. to obtain the invention as specified in claim 9.

As to claim 10, Krivokapic et al. discloses that the body is a fin-type body.

As to claim 11, Krivokapic et al. discloses that the body comprises a patterned silicon-on-insulator structure. The oxide layer is layer (104).

As to claim 14, Kumar discloses (col. 3, lines 8-11 and lines 43-46) that the first double gate (22') receives a first control signal and the second double gate receives a second control signal.

Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic et al. in view of Kumar and further in view of Yu. As to claim 23, Krivokapic et al. in view of Kumar discloses the invention of claim 9, as described above. Krivokapic et al. in view of Kumar does not disclose expressly the body comprising a fin with a width narrow enough to insure a fully depleted channel. Yu, Figure 3, discloses a fin structure (30) (col. 3, line 32) which would have a width narrow enough to insure a fully depleted channel. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the channel of Krivokapic et al. as the fin structure of Yu. The motivation for doing so would have been to construct a device which would used in the sub-0.25-μm gate length regime (Yu, col. 1, line 35). Therefore, it would have been obvious to combine Yu with Krivokapic et al. in view of Kumar to obtain the invention as specified in claim 23.

As to claim 24, Krivokapic et al. discloses that the first side of the body and the second side of the body are on opposite sides of the body.

As to claim 25, Kumar discloses (col. 3, lines 8-11 and lines 43-46) that the first double gate (22') receives a first control signal and the second double gate receives a second control signal.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Kumar. Yu, Figure 3, discloses a method for forming a transistor comprising forming a fin body (35) formed on a substrate, the fin body having a first vertical edge and a second vertical edge. Yu, Figure 6, discloses the fin body formed with a first end and a second end, a source (50) formed at the first end of the fin body and a drain formed at the second end of the fin body. Yu, Figure 6, further discloses a gate structure adjacent the transistor body first vertical edge and second vertical edge. Yu does not disclose expressly a second gate structure. Kumar, Figure 4, discloses a dual double gate FET embodied as a microwave frequency power divider. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form an additional gate structure, of the same form and structure as the disclosed gate structure, in the device of Yu in order to fabricate the circuit of Kumar. One gate structure would necessarily be approximate to the source and the other would be approximate to the drain. The motivation for doing so would have been to construct a device which can divide a power signal among two or more paths (Kumar, col. 1, lines 14-15). Therefore, it would have been obvious to combine Kumar with Yu to obtain the invention as specified in claim 30.

***Allowable Subject Matter***

Claims 12, 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses a plurality of insulating spacers between the first and second portions of the first and second double gates.

Claims 26-29 are allowed. No prior art, including Kumar, discloses insulating spacers formed between the first and second double gates.

Claims 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the first and second double gates formed so that a portion of the first gate structure adjacent to the first vertical edge of the transistor body is directly opposite a portion of the second gate structure adjacent to the second vertical edge of the transistor body.

Claims 35-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses that the edge of the first gate structure adjacent to the first vertical edge of the transistor body is opposite, and displaced less than the body thickness from an edge of the second gate structure adjacent to the second vertical edge of the transistor body.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

srw
February 15, 2006